Amendments to the Drawings:

Applicants submit new sheets comprising Figures 6A and 6B. No new matter is added.

Attachment: New Sheets

REMARKS

Receipt of the Office action of December 20, 2005 is hereby acknowledged. In that action the Examiner: 1) rejected claims 2-4 and 7 as allegedly failing to comply with the enablement requirement; 2) rejected claim 1 as allegedly unpatentable over Park et al. (U.S. Pat. No. 6,832,305) in view of So (U.S. Pat. No. 6,944,746); 3) rejected claims 2-4 and 7 as allegedly unpatentable over Park in view of So in further view of Seal et al. (U.S. Pat. No. 6,965,984); 4) rejected claims 5-6 and 8 as allegedly unpatentable over Park in view of So in further view of Gorishek, IV et al. (U.S. Pat. No. 6,308,255); 5) rejected claims 9-20 as allegedly unpatentable over Park in view of Gorishek, IV; 6) rejected claims 21-26 as allegedly unpatentable over Park in view of So in further view of Gorishek, IV; 7) rejected claims 27-33 as allegedly unpatentable over Park in view of So in further view of Gorishek, IV; 8) objected to the drawings; and 9) objected to the specification.

With this Response, Applicants amend claims 1-2, 9, 11-14, 21, and 27. Applicants believe the pending claims are allowable over the art of record and respectfully request reconsideration.

I. AMENDMENTS TO THE SPECIFICATION

With respect to paragraphs [0001], [0024]-[0025], [0029], and [0033], Applicants present a plurality of amendments to add serial numbers and/or patent numbers of related cases, and to correct grammatical shortcomings. Applicants also add paragraphs to address the drawing objections, discussed immediately below. No new matter is added.

II. DRAWING OBJECTIONS

The Office action objects to the drawings for various informalities. To address these concerns, Applicants present Figures 6A and 6B, as well as corresponding paragraphs [0012.1], [0012.2], [0036.1] and [0036.2]. As for Figure 6A and paragraph [0036.1], the figure and paragraph find support in the original disclosure at claims 2-4 and 9-20, as well as the original specification paragraphs [0024] and [0026]-[0030]. As for Figure 6B and paragraph [0036.2], the figure and paragraph find support in the original

disclosure at claims 21-33, as well as the original specification paragraphs [0003], [0024], [0026]-[0030], and [0032]-[0036]. No new matter is added.

III. 35 U.S.C. § 112, 1ST PARAGRAPH-BASED REJECTIONS

Claims 2-4 and 7 stand rejected as allegedly failing to comply with the enablement requirement.

Regarding claims 3 and 4, Applicants respectfully traverse. The Examiner argues as to inclusion of the limitation "Java Impdep1 Bytecode". Claims 3 and 4, however, do not recite this limitation. Instead, claims 3 and 4 specifically recite, "Java bytecode". Moreover, the term "Java bytecode" is common to those of ordinary skill in the art (e.g., Attachment: Haggar, Peter. Java Bytecode [online]. IBM, July 1, 2001 [retrieved on 2006-07-28]. Retrieved from the Internet: <URL: http://www-128.ibm.com/developerworks/ibm/library/it-haggar_bytecode/>). Applicants respectfully submit that in view of the specific recitation of claims 3 and 4, the available public knowledge, and the support found in the original disclosure at paragraphs [0016] and [0028], claims 3 and 4 are fully enabled, and the rejections should be withdrawn.

Regarding claims 2 and 7, Applicants respectfully traverse. The Examiner argues as to the limitation "Java Impdep1 Bytecode". Paragraph [0028] of the original disclosure specifically recites, "Java reserved code such as the 'Impdep1' Bytecode". Further, paragraph [0035] of the original disclosure specifically recites, "the Java instruction set may include two Java implementation dependent and reserved codes, e.g., Impdep1 and Impdep2". Applicants submit that these descriptions of the Java Impdep1 Bytecode provided in the original disclosure, together with the available public knowledge, fully enable one of ordinary skill in the art. For example, Lindholm and Yellin (Attachment: Lindholm, Tim and Yellin, Frank. The Java Virtual Machine Specification Second Edition [online]. Sun Microsystems, Inc., 1999 [retrieved on 2006-07-28]. Retrieved from the Internet: <URL: http://java.sun.com/docs/books/vmspec/2nd-edition/html/Instructions.doc.html>) provide a description of the Impdep1 and Impdep2 reserved bytecodes. Further, the Byte Code Engineering Library (Attachment: jakarta-bcel 5.2 API [online]. Apache Software Foundation, 2002-2006 [retrieved on 2006-07-28]. Retrieved from the Internet: <URL: http://jakarta.apache.org/bcel/apidocs/org/

apache/bcel/generic/IMPDEP1.html>) provides a description of the Java Impdep1 Bytecode including field, constructor, and method summaries as well as constructor and method details, which provide information as to the usage of the Java Impdep1 Bytecode. Based on the foregoing, Applicants submit that claims 2 and 7 are fully enabled, and the rejections should be withdrawn.

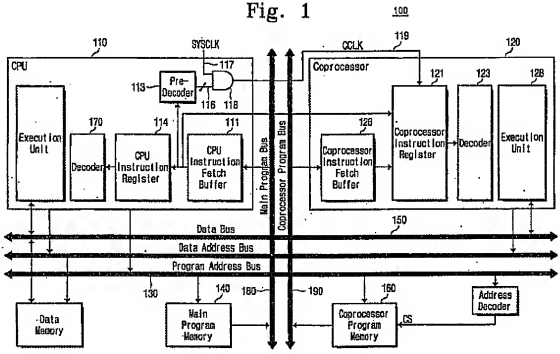
IV. ART-BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly unpatentable over Park in view of So. Applicants respectfully traverse.

Park is directed to method and apparatus for executing coprocessor instructions (Park Title). In particular and in relevant part, Park appears to disclose a data processing system having a main processor that executes CPU instructions and a coprocessor that executes coprocessor instructions (Park Col. 3, lines 25-30). The main processor fetches and decodes instructions from a main program memory and the coprocessor fetches and decodes instructions from a coprocessor program memory (Park Col. 3, lines 38-67 and Col. 4, lines 1-30). Thus, Park teaches a **dual processor system**, comprising the main processor and the coprocessor, **which separately decode two instruction sets**. The dual processor system is best illustrated in Park's Figure 1, reproduced immediately below:

Fig. 1



Referring specifically to the main processor (element 110) and the coprocessor (element 120), the system comprises two processors each comprising their own decoders (element 170 and element 123, respectively) used for separately decoding two instruction sets.

So is directed to RISC processor supporting one or more uninterruptible co-processors (So Title). In particular and in relevant part, So appears to disclose a computer system comprising a system having a core microprocessor and a coprocessor (So Col. 3, lines 48-60). The core microprocessor analyzes and executes non-coprocessor instructions (So Col. 8, lines 24-31), and the coprocessor analyzes and executes coprocessor instructions (So Col. 7, lines 20-21 and Col. 8, lines 31-42). Thus, So also teaches **a dual processor system**, comprising the core microprocessor and the coprocessor, **which separately analyze two instruction sets**.

Claim 1, by contrast, specifically recites, "**A processor, comprising: decode logic adapted to decode instructions from a first instruction set** in a first mode **and adapted to decode instructions from a second instruction set** in a second mode". Applicants respectfully submit that Park and So do not expressly or inherently teach such a system. The Office Action relies on So's alleged teaching of a single decoder on a single processor that decodes multiple instruction sets. The reliance is misplaced. So's core microprocessor provides a pre-analyze function for both instruction sets inasmuch as it identifies the two different instruction sets (So Col. 7, lines 3-21); however, So clearly teaches execution of core microprocessor commands and coprocessor commands based on separate analyzing (within each processor) and execution of two different instruction sets. Thus, Park and So fail to teach or suggest "**A processor, comprising: decode logic adapted to decode instructions from a first instruction set** in a first mode **and adapted to decode instructions from a second instruction set** in a second mode".

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 2-8), should be allowed. Applicants amend claims 1 and 2 to correct grammatical deficiencies. No new matter is added.

B. Claim 9

Claim 9 stands rejected as allegedly unpatentable over Park in view of Gorishek, IV. Applicants amend claim 9 to more clearly define over Park's multiple decoders and to correct grammatical deficiencies. The amendment finds support in the original specification at Paragraphs [0024] and [0026], and Claim 9.

Park teaches a dual processor system, comprising the main processor and the coprocessor, which separately decode two instruction sets. In particular and in relevant part, Park's system comprises **two decoders used for separately decoding two instruction sets** (Park Figure 1, element 170 and element 123). Gorishek, IV is directed to symmetrical multiprocessing bus and chipset used for coprocessor support allowing non-native code to run in a system (Gorishek, IV Title). The Office Action has relied on Gorishek, IV only for a teaching of switching the decoding permanently from one mode to another.

Claim 9, by contrast, specifically recites, "wherein the **decoding of both instruction sets is performed on a single decoder**". Applicants respectfully submit that Park and Gorishek, IV do not expressly or inherently teach such a system. In particular, it appears that the Park system calls for **two decoders used for separately decoding two instruction sets**. Thus, even if the teachings of Gorishek, IV are precisely as the Office Action suggests (which Applicants do not admit), Park and Gorishek, IV still do not teach, and in fact appear to teach away from, a system "wherein the **decoding of both instruction sets is performed on a single decoder**".

Based on the foregoing, Applicants respectfully submits that claim 9, and all claims which depend from claim 9 (claims 10-20), should be allowed. Applicants amend claims 11-14 to correct grammatical deficiencies. No new matter is added.

C. Claim 21

Claim 21 stands rejected as allegedly unpatentable over Park in view of So in further view of Gorishek, IV. Applicants respectfully traverse.

Park teaches a **dual processor system**, comprising the main processor and the coprocessor, **which separately decode two instruction sets**. Similarly, So teaches **a dual processor system**, comprising the core microprocessor and the coprocessor,

which separately analyze two instruction sets. The Office Action has relied on Gorishek, IV only for a teaching of switching the decoding permanently from one mode to another.

Claim 21, by contrast, specifically recites, "**A processor, comprising: decode logic adapted to decode instructions from a first instruction set** in a first mode **and adapted to decode instructions from a second instruction set** in a second mode". Applicants respectfully submit that Park, So, and Gorishek, IV do not expressly or inherently teach such a system. The Office Action relies on So's alleged teaching of a single decoder on a single processor that decodes multiple instruction sets. The reliance is misplaced. So's core microprocessor provides a pre-analyze function for both instruction sets inasmuch as it identifies the two different instruction sets (So Col. 7, lines 3-21); however, So clearly teaches execution of core microprocessor commands and coprocessor commands based on separate analyzing (within each processor) and execution of two different instruction sets. Thus, even if the teachings of Gorishek, IV are precisely as the Office Action suggests (which Applicants do not admit), Park, So, and Gorishek, IV still do not teach, and in fact appear to teach away from, "**A processor, comprising: decode logic adapted to decode instructions from a first instruction set** in a first mode **and adapted to decode instructions from a second instruction set** in a second mode".

Based on the foregoing, Applicants respectfully submit that claim 21, and all claims which depend from claim 21 (claims 22-26), should be allowed. Applicants amend claim 21 to correct grammatical deficiencies. No new matter is added.

D. Claim 27

Claim 27 stands rejected as allegedly unpatentable over Park in view of So in further view of Gorishek, IV. Applicants respectfully traverse.

Park teaches a **dual processor system**, comprising the main processor and the coprocessor, **which separately decode two instruction sets**. Similarly, So teaches **a dual processor system**, comprising the core microprocessor and the coprocessor, **which separately analyze two instruction sets**. The Office Action has relied on

Gorishek, IV only for a teaching of switching the decoding permanently from one mode to another.

Claim 27, by contrast, specifically recites, "**the co-processor comprising: decode logic adapted to decode instructions from a first instruction set** in a first mode **and adapted to decode instructions from a second instruction set** in a second mode". Applicants respectfully submit that Park, So, and Gorishek, IV do not expressly or inherently teach such a system. The Office Action relies on So's alleged teaching of a single decoder on a single processor that decodes multiple instruction sets. The reliance is misplaced. So's core microprocessor provides a pre-analyze function for both instruction sets inasmuch as it identifies the two different instruction sets (So Col. 7, lines 3-21); however, So clearly teaches execution of core microprocessor commands and coprocessor commands based on separate analyzing (within each processor) and execution of two different instruction sets. Thus, even if the teachings of Gorishek, IV are precisely as the Office Action suggests (which Applicants do not admit), Park, So, and Gorishek, IV still do not teach, and in fact appear to teach away from, "**the co-processor comprising: decode logic adapted to decode instructions from a first instruction set** in a first mode **and adapted to decode instructions from a second instruction set** in a second mode".

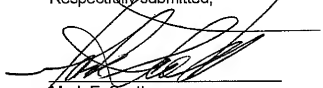
Based on the foregoing, Applicants respectfully submit that claim 27, and all claims which depend from claim 27 (claims 28-33), should be allowed. Applicants amend claim 27 to correct grammatical deficiencies. No new matter is added.

V. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,



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